WHAT IS CLAIMED IS:

1. A method for manufacturing a semiconductor device, comprising:

forming a conductive layer on a first insulating layer formed on a substrate, and on a plurality of contact plugs formed in the first insulating layer;

forming a plurality of capacitor element lower electrodes by patterning the conductive layer;

forming a second insulating layer on the first insulating layer and the capacitor element lower electrodes;

forming a recess in the second insulating layer at a region above the capacitor element lower electrodes;

planarizing the second insulating layer by polishing;

exposing the capacitor element lower electrodes; and

forming a capacitive insulating film and capacitor element upper electrodes above the capacitor element lower electrodes.

2. The method for manufacturing a semiconductor device according to claim 1, wherein the step of exposing the capacitor element lower electrodes is carried out by etchback.

3. The method for manufacturing a semiconductor device according to claim 2, wherein the step of planarizing the second insulating layer by polishing is carried out by CMP (chemical mechanical polishing).

4. The method for manufacturing a semiconductor device according to claim 1, wherein the step of planarizing the second insulating layer by polishing and the step of exposing the capacitor element lower electrodes are carried out by a single step for planarization and exposure.

5. The method for manufacturing a semiconductor device according to claim 4, wherein the step for planarization and exposure is carried out by CMP.

6. The method for manufacturing a semiconductor device according to claim 1, wherein in the step of forming capacitor element lower electrodes, metal conductors are formed together with the capacitor element lower

electrodes by patterning the conductive layer.

7. The method for manufacturing a semiconductor device according to claim 6, wherein recesses in the second insulating layer are formed only in a region in which the capacitor element lower electrodes are arranged.

8. The method for manufacturing a semiconductor device according to claim 1, wherein the surface of the conductive layer is made of Pt, Ir, Ru, an alloy thereof or a metal oxide thereof.

9. The method for manufacturing a semiconductor device according to claim 1, wherein the step of forming a recess in the second insulating layer is performed by dry etching.

10. The method for manufacturing a semiconductor device according to claim 9, wherein a depth of the recess formed in the second insulating layer is substantially the same as a film thickness of the capacitor element lower electrodes.

11. The method for manufacturing a semiconductor device according to claim 9, wherein at least a portion of the capacitor element lower electrodes is exposed during the formation of the recess in the second insulating film.

12. The method for manufacturing a semiconductor device according to claim 9, wherein the dry etching is performed such that a taper angle of less than 90° is formed at a bottom corner of the recess formed in the second insulating layer.

13. The method for manufacturing a semiconductor device according to claim 1, wherein the second insulating film is an SiO_2 film formed by atmospheric CVD using ozone and tetraethylorthosilicate.

14. The method for manufacturing a semiconductor device according to claim 1, wherein a region of the recess of the second insulating layer is made larger than the capacitor element lower electrodes below that region.

15. The method for manufacturing a semiconductor device according to

claim 1, wherein the recess of the second insulating layer is formed at a size spanning a region above a plurality of the capacitor element lower electrodes.

16. A semiconductor device, comprising:

a substrate;

a first insulating layer formed on the substrate;

a contact plug formed in the first insulating layer;

a capacitor element lower electrode formed on the first insulating layer and connected to the contact plug;

a second insulating layer formed burying the capacitor element lower electrode and its surroundings;

a capacitive insulating film formed covering the capacitor element lower electrode; and

a capacitor element upper electrode formed above the capacitor element lower electrode with the capacitive insulating film interposed in between, such that the capacitor element lower electrode becomes a capacitance-defining area,

wherein a plurality of capacitor elements composed of the capacitor element lower electrode, the capacitive insulating film and the capacitor element upper electrode are arranged in a capacitor element group, and

wherein a surface of the capacitor element lower electrodes and the second insulating layer is planarized by polishing, and a surface area of the capacitor element group is within the range of 10,000 to 100,000 μm^2.

17. The semiconductor device according to claim 16, wherein a plurality of the capacitor element groups are provided, and a spacing between adjacent capacitor element groups is within the range of 10 to 100 μm.